Amendments to the Claims:

1. (previously presented) A method for clock generation and distribution in an emulation system comprising:

generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal;

stopping emulation by stopping the base clock signal, wherein the index to the look up table is stopped at a stopping point in a clock cycle of the derived clock signal and the derived clock signal does not continue to a subsequent transition before stopping; and

resuming emulation by resuming the base clock signal, wherein the derived clock signal is resumed at the stopping point in the clock cycle of the derived clock signal.

2. (previously presented) The method of claim 1, wherein generating the derived clock signal further comprises:

accessing an entry in a look up table having an address corresponding to a number of clock cycles that have been counted; and

outputting a signal level in response to the entry accessed.

3. (currently amended) An emulation system comprising:

a plurality of emulation boards each having hardware to emulate one or more circuit designs;

means for interconnecting the plurality of emulation boards;

a clock generation circuit to stop and resume emulation of the one or more circuit designs comprising

a base clock generation circuit that generates a base clock signal of a first frequency, and

a derived clock generation circuit having

a frequency divider circuit coupled to receive the base clock signal,

a counter circuit coupled to receive an output of the frequency divider circuit, and

a look up table coupled to receive an output of the counter circuit, wherein the output of the counter circuit is used to index entries in the look up table, and further wherein the entries in the look up table indicate a signal level for a derived clock signal generated by the clock generation circuit, wherein when the base clock signal is stopped, the derived clock signal is stopped at a stopping point in a clock cycle of the derived clock signal without continuing to a subsequent transition of the derived clock signal, and the derived clock signal is resumed from the stopping point when the base clock signal is resumed.

4. (previously presented) The emulation system of claim 3, further comprising a plurality of additional clock generation circuits coupled in parallel to generate a plurality of additional derived clock signals.

5. (previously presented) The emulation system of claim 4, wherein the plurality of additional clock generation circuits each further comprise a selection circuit comprising a multiplexor coupled to receive the base clock signal and to receive an external clock signal from an external source, the multiplexor having an output coupled to a respective frequency divider circuit, wherein a select input of the multiplexor is provided by the external source.

6. (previously presented) The emulation system of claim 5, wherein the plurality of additional clock generation circuits each further comprise a frequency multiplier circuit that multiplies the external clock signal and provides a multiplied external clock signal to the multiplexor.

7. (previously presented) The emulation system of claim 3, wherein the derived clock signal is distributed to the plurality of emulation boards.

8. (previously presented) An apparatus for generating clock signals in an emulation system comprising:

means for generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal;

means for stopping emulation by stopping the base clock signal, wherein the index to the look up table is stopped at a stopping point in a clock cycle of the derived clock signal and the derived clock signal does not continue to a subsequent transition before stopping; and

means for resuming emulation by resuming the base clock signal, wherein the derived clock signal is resumed at the stopping point in the clock cycle of the derived clock signal.

9. (previously presented) The apparatus of claim 8, wherein the means for generating a derived clock signal further comprises:

means for accessing an entry in a look up table having an address corresponding to a number of clock cycles that have been counted; and

means for outputting a signal level in response to the entry accessed.

10.-13. (canceled)

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14. (currently amended) An apparatus for generating a derived clock signal, the apparatus comprising:

a counter to count cycles in a base clock signal and to provide a counter output corresponding to a number of counted cycles;

a look up table to receive the counter output as a sequence of indexes and to output a sequence of signal values from entries in the look up table that correspond to the sequence of indexes, said sequence of signal values comprising the derived clock signal; and

a multiplexor to receive a first signal and a second signal and to selectively provide one of the first signal and the second signal to the counter as the base signal, ~~The~~

~~apparatus of claim 13~~ wherein the multiplexor provides one of the first signal and the second signal to the counter through a frequency divider.

15. (currently amended) An apparatus for generating a derived clock signal, the apparatus comprising:

a counter to count cycles in a base clock signal and to provide a counter output corresponding to a number of counted cycles;

a look up table to receive the counter output as a sequence of indexes and to output a sequence of signal values from entries in the look up table that correspond to the sequence of indexes, said sequence of signal values comprising the derived clock signal; and ~~The apparatus of claim 10 further comprising:~~

a frequency multiplier to multiply a first signal up to the base signal and to provide the base signal to the counter.

16. (previously presented) The apparatus of claim 15 wherein the frequency multiplier provides the base signal to the counter through at least one of a multiplexor and a frequency divider.

17.-20. (canceled)